UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/563,509	01/05/2006	Tomohiro Uryu	MAT-8791US	8639

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RATNERPRESTIA
P.O. BOX 980
VALLEY FORGE, PA 19482

EXAMINER
WILLIS, RANDAL L

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PTOL-90A (Rev. 04/07)

APPLICATION NO./ CONTROL NO.	FILING DATE	FIRST NAMED INVENTOR / PATENT IN REEXAMINATION	ATTORNEY DOCKET NO.
10/563,509	05 January 2006	URYU ET AL.	MAT-8791US

RATNERPRESTIA
P.O. BOX 980
VALLEY FORGE, PA 19482

EXAMINER
RANDAL WILLIS

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Commissioner for Patents

Examiner's Answer to Appeal Brief mailed 5/19/2011 now correctly lists the filing date of the appeal brief as 3/07/2011

PTO-90C (Rev.04-03)

BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/563,509
Filing Date: January 05, 2006
Appellant(s): URYU ET AL.

Lawrence E. Ashery
<u>For Appellant</u>

EXAMINER'S ANSWER

This is in response to the appeal brief filed 3/07/2011 appealing from the Office action

mailed 8/23/2010.

(1) Real Party in Interest

The examiner has no comment on the statement, or lack of statement, identifying by name the real party in interest in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The following is a list of claims that are rejected and pending in the application:
Claims 1-6.

(4) Status of Amendments After Final

The examiner has no comment on the appellant's statement of the status of amendments after final rejection contained in the brief.

(5) Summary of Claimed Subject Matter

The examiner has no comment on the summary of claimed subject matter contained in the brief.

(6) Grounds of Rejection to be Reviewed on Appeal

The examiner has no comment on the appellant's statement of the grounds of rejection to be reviewed on appeal. Every ground of rejection set forth in the Office action from which the appeal is taken (as modified by any advisory actions) is being maintained by the examiner.

(7) Claims Appendix

The examiner has no comment on the copy of the appealed claims contained in the Appendix to the appellant's brief.

(8) Evidence Relied Upon

20040263496	Miura	12-2004
5200738	Fumoto	4-1993
WO/03044766	Miura	5-2003

Black, Ken "What is Asynchronous Transfer Mode" (2003)

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* v. *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 1-6 are rejected 35 U.S.C. 103(a) as obvious over Miura (WO03044766

in which US2004/0263496 will be used as an English translation) in view of Fumoto

(5200738) and "What is Asynchronous Transfer Mode" by Ken Black.

Apropos claim 1, Miura teaches:

An image signal processing device comprising:

a semiconductor integrated circuit (42, Fig. 3) having:

a video signal processing unit for outputting video output data to a display device

in a plurality of fields (Image controller 42b, Fig. 3); and

a control unit for holding data for controlling an operation of the video signal

processing unit (42a holds data for the image controller, Fig. 3); and

an external memory (41, Fig. 3) that is disposed outside the semiconductor

integrated circuit, holds control data to be fed to the control unit ([0049]) and allows data

read to be controlled by the control unit,

wherein data transferred between the external memory and the control unit has

data that must be updated in every field of the plurality of fields and data that does not

need to be updated in every field of the plurality of fields(Data held is dynamic which is

updated and static which is not, [0050] and [0051]), and

the data that does not need to be updated in every field is divided into a plurality

of reduced size data, the plurality of reduced size data assigned to the plurality of fields

respectively, and transferred (See Fig. 4b, static control data divided into fields such as

15a-c).

However, Miura doesn't explicitly teach:

The data is transferred in a vertical blanking time period of the video output data

And the reduced size data having a common size corresponding to a length of

the vertical blanking time period.

In the same field of transferring data within display devices, Fumoto teaches

transferring data to the display from an external memory during the vertical blanking

period of the display device (Col 4 lines 30-40).

Therefore it would have been obvious to one of ordinary skill in the art at the time

of the invention to have the data transfer of Miura occur during the vertical blanking

period as taught by Fumoto in order to not disrupt the displaying of the image on the

display device, this would have the obvious consequence of the data to be sent must be

divided into small enough segments to be sent in each vertical blanking period.

Further Black teaches a method of transferring data where the data is divided

into a plurality of cells, each cell being the same bit length in order to create a very

efficient way to transfer video data and speed up the data transmission.

Therefore it would have been obvious to one of ordinary skill in the art at the time

of the invention to ensure that the reduced sized data of Miura was reduced to a fixed

data length as taught by Black so that less resources need to be used to denote the

beginning and ending of the data sent and thus speed up the data transmission.

Apropos claim 2, Miura teaches:

The image signal processing device according to claim 1, wherein the video signal processing unit has a memory for holding the data that must be updated every field and a memory for holding the data that does not need to be updated every field (Dynamic and Static control data both delivered to 42, See Fig. 3 and [0071]).

Apropos claim 3, Miura and Fumoto teaches:

Wherein the data is divided into the plurality of reduced size data to ensure that each one of the plurality of data can be transferred between the external memory and the control unit, respectively during successive vertical blanking periods (Miura's teaching of dividing the data into a plurality of frames combined with Fumoto's teaching of using the vertical blanking period to transfer the data would inherently have to insure that data sent during a vertical blanking period was short enough to be successfully sent during the time required).

Apropos claim 4, Miura teaches:

An image signal processing device for a display device performing a display according to a subfield driving method comprising:

a semiconductor integrated circuit having:

a video signal processing unit for outputting video output data to the display device in a plurality of fields (Image controller 42b, Fig. 3);

a control unit for holding data for controlling an operation of the video signal processing unit (42a holds data for the image controller, Fig. 3);

an external memory (41, Fig. 3) that is disposed outside the semiconductor

integrated circuit, holds control data to be fed to the control unit ([0049]) and allows data

read to be controlled by the control unit,

wherein the video signal processing unit includes:

an image quality correcting circuit for signal processing to correct image quality

of video signal data input in the video signal processing unit (42ba, Fig 8)

a subfield converting circuit (42bb, Fig. 8) for generating a signal for every

subfield of the plurality of fields based on output data from the image quality correcting

circuit,

a first memory for holding data, that must be updated in every field of the plurality

of fields, required by the image quality correcting circuit (42a receives dynamic control

data from 41a, Fig. 8), and

a second memory for holding data, that does not need to be updated in every

field of the plurality of fields, required by the subfield converting circuit (44a receives

static control data from 41b, Fig. 8),

wherein the semiconductor integrated circuit has a plurality of terminals and at

least two of the plurality of terminals are used for both outputting the video output data

output from the video signal processing unit and transferring data between the external

memory and the control unit (See connections in Fig. 8 showing both connections to the

memory banks, and video data output), and

the data transferred between the external memory and the control unit has data

that must be updated in every field of the plurality of fields and data that does not need

to be updated in every field of the plurality of fields(Data held is dynamic which is

updated and static which is not, [0050] and [0051]), and

data stored in the external memory in the vertical blanking time period are

acquired into the second memory for holding the data required by the subfield

converting circuit in every field and an operation of the subfield converting circuit is

controlled based on the data ([0063] and [0069] and [0074])

the data that does not need to be updated in every field is divided into a plurality

of reduced size data, the plurality of reduced size data assigned to the plurality of fields

respectively, and transferred (See Fig. 4b, static control data divided into fields such as

15a-c).

However, Miura fails to explicitly teach:

data stored in the external memory can be ROM data

The data is transferred in a vertical blanking time period of the video output data

In the same field of transferring data within display devices, Fumoto teaches

transferring data to the display from an external memory during the vertical blanking

period of the display device (Col 4 lines 30-40)

The data that does not need to be updated in every field is divided into a plurality

of data having a common size corresponding to a length of the vertical blanking time

period.

Therefore it would have been obvious to one of ordinary skill in the art at the time

of the invention to have the data transfer of Miura occur during the vertical blanking

period as taught by Fumoto in order to not disrupt the displaying of the image on the display device.

Further Black teaches a method of transferring data where the data is divided into a plurality of cells, each cell being the same bit length in order to create a very efficient way to transfer video data and speed up the data transmission (Paragraph 3).

Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to ensure that the reduced sized data of Miura was reduced to a fixed data length as taught by Black so that less resources need to be used to denote the beginning and ending of the data sent and thus speed up the data transmission.

Further, Examiner takes official notice that the use of ROM and RAM in display devices is well known to one of ordinary skill in the art at the time of the invention, and therefore the use of ROM data for data that doesn't need to be changed in the memory of Miura would have been obvious to one of ordinary skill in the art at the time of the invention in order to prevent accidental erasure of important data.

Apropos claim 5, Miura teaches:

Wherein a line for outputting the video output data is connected with a line for outputting the data output from the external memory (VD2 is connected through the image control 42 to the outputs of 41, which are the data output from the external memory, Fig. 3).

Apropos claim 6, Miura and Fumoto teach:

Wherein the data that does not need to be updated in every field is divided into a plurality of reduced size data ([0087]) corresponding to a length of the vertical blanking time period (Fumoto teaches transferring data in vertical blanking period Col 4 lines 30-40, thus the size of the data frames of Miura would inherently have to be small enough to transmit during the vertical blanking period), the plurality of reduced size data assigned to the plurality of fields respectively, and transferred.

(10) Response to Argument

Appellant argues that one of ordinary skill in the art would not modify Miura to divide the data based on a common size, due to Miura's teaching of transferring each type of data at the same time, which would not necessarily have the same common size. However, one of ordinary skill in the art would have found it obvious that a transmission of data can be broken into smaller packets of data for transfer, and reassembled at the destination, in such cases where the time frame for sending the data was smaller than the time required to transfer the allotted data. It would then be obvious that a common transfer protocol such as the ATM method, which divides the data to be sent into smaller packets of a predetermined (and therefor common) size, shown by Black could be used to achieve the predictable result of transfer the data in pieces to arrive at the destination.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the

Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

Randal Willis

/Randal Willis/

Examiner, Art Unit 2629

Conferees:

Amare Mengistu

/Amare Mengistu/

Supervisory Patent Examiner, Art Unit 2629

/Bipin Shalwala/

Supervisory Patent Examiner, Art Unit 2629